REMARKS

Claims 1-4 and 7 and 8 are claims presently pending in this case.

Favorable reconsideration and allowance of the claims of the present application, as amended, is respectfully requested.

In the present Office Action, now a FINAL REJECTION, the Examiner rejected Claims 1-4, 7 and 8 under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Publication No. 2004/0222859 to Hajimiri, et al. ("Hajimiri"). As the Hajimiri reference was never cited against the claims of the present invention, this amendment addressing the pertinence of Hajimiri, could not have earlier been presented. Applicants respectfully request entry of the following.

With respect to the rejections of independent Claim 1 as being anticipated by Hajimiri, applicants respectfully disagree. The present invention is directed to a vertically stacked coplanar transmission line structure for an integrated circuit (IC) chip forming each of two structures comprising the microstrip pair. Present Claim 1 is being amended herein to clarify the stacked coplanar transmission line structures of the micro-strip pair are separated by a distance. No new matter is being entered by this amendment as clear support is found in the specification, e.g., on page 4 paragraph [0019] and in Figures 1 and 3. As claimed, each stacked coplanar transmission line structure of the pair comprises: a metal layer, a next metal layer down, and an intermediate connecting via layer in between the metal layer and the next metal layer down, the intermediate connecting via layer comprising a via bar having a width dimension

approximately equal to a width dimension of the first and second vertically stacked coplanar conductors and having a length dimension approximately equal to a length dimension of said first and second vertically stacked coplanar conductors.

Respectfully, Hajimiri does not meet any of the limitations of the Claim 1 as amended.

In the rejection of Claim 1, the Examiner alleges that Hajimiri teaches a microstrip pair of vertically stacked coplanar transmission line structure for an IC (integrated circuit chip). Applicants respectfully disagree.

First of all, Hajimiri is directed to the field of distributed oscillators, particularly, oscillators that will be integrated within an IC. However, Hajimiri's device is not a microstrip pair of transmission line structures. The fact that Hajimiri's device is incorporated in an IC is where any degree of similarity ends. The Examiner, in the final rejection, nonetheless indicates that page 3, paragraph [0028] of Hajimri coupled with the accompanying drawings of Figures 5A-5B, allegedly anticipates Claim 1 as amended.

It is respectfully submitted that the Examiner, while entitled to a broad reading of the claims, misinterprets the Hajimiri by indicating that it is a microstrip structure. Respectfully, in transmission line theory, a micro-strip pair has a specific meaning and structure for generating electric field patterns associated with non-TEM (transverse electromagnetic mode) of signal propagation.

To the contrary, Hajimiri is directed to an oscillator structure comprising a four (4) port structure having two transmission lines each with an amplifier device interconnecting the two transmission lines. The Examiner particularly cites Hajimiri page 3, parag. [0028] and the

teachings of Figure 5A and 5B as teaching the present invention. However, respectfully, Hajimiri does not provide a microstrip structure having two stacked coplanar transmission line structures of the micro-strip pair are separated by a distance. Rather, Hajimiri provides a structure that functions as an oscillator and, does not provide a conductive via layer in intermediate connection with the top metal layer and underlying metal layer in each vertically stacked structure of the microstrip pair as claimed in the present invention. Hajimiri rather discusses an input transmission line (conductor 602 in Figure 5A of Hajimiri) and an output transmission line (conductor 604) shown interconnected with an amplifier device (transistor 608) forming distributed oscillator 612. A further transmission line (third transmission line 606) is interconnected with the second transmission line 604 by a further amplification device (transistor 610).

The Examiner in the Office Action rejection further likens the middle transmission line (element 604) in Figure 5A as an intermediate connecting via layer in between two metal layers 606 and 602. However, respectfully, this is not an interconnecting via as contemplated and taught in the present invention and claimed in Claim 1. The term via has associated meaning to a skilled artisan as a passive conductor layer that interconnects two conductor (metal) layers and electrically couples the metal layers. A via layer is not a transmission line. In the present invention, the microstrip pair comprises a first vertical stack and a second vertical stack in a coplanar configuration, each vertical stack having two layers of metal and an interconnecting via metal layer therebetween comprising a via bar. In Hajimiri, the layer that the Examiner likens the claimed via bar in Claim 1 to the output transmission line 604 (Hajimiri, Figure 5A) that couples the two transmission lines via active devices (amplifiers 608,

610). Thus, the Examiner's characterization of Hajimiri's layer 604 as a via layer is respectfully incorrect.

Moreover, in Hajimiri, the trio of conductors transmission lines 602, 604 and 606, do not form a stacked structure (the word "stack" does not appear in the Hajimiri at all) and is contrary to the typically meaning of a stack as known to skilled artisans familiar with CMOS device manufacturing technology.

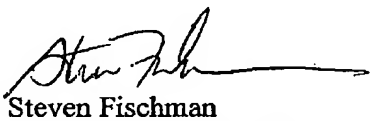
Moreover, even though the Hajimiri's Figures 5A show approximately equal width and length dimensions for each transmission line (602, 604 and 606) shown in Figure 5A, it is respectfully submitted that Hajimiri disclosure is actually silent as to the length and width dimensions of each transmission line. The dimensions of these transmission lines 602, 604 and 606 are presented similar in dimension for purposes of illustration and, in fact, appear to extend further out as indicated by the dashed lines at each end. Thus, it can not be relied on for certainty that Hajimiri teaches structures having equal width and length. In fact, the discussion of Hajimiri on page 3, paragraph [0031] indicates that embodiments for the distributed oscillator may take the form of straight, square, and polyhedron or other suitable shapes /configurations.

In view of the foregoing, the Examiner is respectfully requested to withdraw the rejection of Claims 1-4, 7, 8 as being anticipated by Hajimiri.

In view of the foregoing amendments and remarks, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If

the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicants' attorney at (516) 742-4343.

Respectfully submitted,



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